REMARKS

Claims 1, 3, 5-10, and 12-16 remain in the application and stand rejected. Reconsideration of the rejection is respectfully requested in light of the following reasons.

Rejection -- 35 U.S.C. 112

Claims 9-12 and 14-16 stand rejected under 35 U.S.C. §112, paragraph two, as being indefinite. Claim 9 has been amended to further define "high temperature," while claim 15 has been amended to further define "low temperature." Accordingly, it is believed that claims 9-12 and 14-16 now meet the requirements of 35 U.S.C.§112.

Rejections Based on References

The claimed invention pertains to the fabrication of MEMS devices with integrated transistors. The claimed invention provides a process that allows a MEMS device to be fabricated using a high temperature process without substantially degrading a previously formed transistor.

As the last office action suggests, deposition of silicon nitride at high temperatures is well known. However, that is not the gist of the claimed invention. Although high temperature deposition of silicon nitride is well known, such a deposition process previously cannot be used to fabricate a MEMS device after a transistor has already been fabricated. This is because transistors include features that will be degraded when exposed to such high temperatures. The Examiner is respectfully requested to consider this aspect and advantage of the present invention in the following rejections.

Franke and Fiorini

Claims 1, 6, 7, and 8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,448,622 to Franke et al. ("Franke") in view of U.S. Patent No. 6,884,636 to Fiorini et al. ("Fiorini"). The rejection is respectfully traversed.

There are three requirements to establish a prima facie case of obviousness. First, there must be some suggestion or motivation to modify a reference or to combine references. Second, there must be a reasonable expectation of success. Third, the prior art reference or combined references must teach or suggest all the claim limitations. See MPEP § 2143.

Claim 1 recites in part: "forming a first protective layer over a gate, source, and drain of the transistor; and forming a micro-electro-mechanical system (MEMS) structure over the first protective layer, the MEMS structure including a movable element that is formed using a deposition process at a temperature greater than about 700°C." The plain language of claim 1 requires formation of the MEMS structure over the first protective layer, which is formed over the transistor. The MEMS structure is thus formed after the transistor. Furthermore, claim 1 requires the MEMS structure to have a movable element that is formed at a temperature greater than 700°C.

As noted in the last office action, Franke does not disclose forming a MEMS movable element at a temperature of at least 700°C. This is not surprising given that the gist of Franke is to form MEMS structures using low temperature processes. Franke proposes to do so by replacing poly-Si with poly-SiGe in the fabrication of MEMS structures (Franke, col. 4, lines 32-35). At a deposition temperature of 650°C or less, about 550°C to even 325°C (Franke, col. 5, lines 8-22), poly-SiGe deposition can hardly be called a high temperature process. Franke specifically avoids high temperature processes – hence the use of poly-SiGe.

The last office action now proposes to modify Franke with Fiorini. Fiorini discloses that poly-SiGe may be deposited at a temperature between 600°C to 700°C. Fiorini thus teaches deposition of poly-SiGe at most, rather than at least, 700°C. In fact, Fiorini teaches that poly-SiGe is preferably deposited at 650°C (Fiorini, col. 8, lines 35-40). That is, deposition temperature of 700°C is at the far end of Fiorini's process window. As noted above, Franke itself advises to deposit poly-SiGe at a temperature of 650°C or less (Franke, col. 5, lines 14-16). In other words, not only is 700°C at the far end of Fiorini's process window, it is outside of Franke's process window.

It is respectfully submitted that one of ordinary skill in the art reading Franke and Fiorini would not be motivated to modify Franke's process to deposit poly-SiGe at a temperature of at least 700°C because that is outside Franke's process window, and is above the melting point of unprotected metal interconnects used in Franke's device, such as copper or aluminum (Franke, col. 1, lines 39-43; col. 6, lines 7-10). That is, the proposed combination would result in degradation of Franke's device and is in direct contradiction to Franke's advice against high temperature processing, deposition of poly-SiGe above 650°C in particular.

In any event, to expedite prosecution, claim 1 has been amended to recite that the MEMS movable element is formed using a deposition process at a temperature greater than about 700°C. Neither Franke nor Fiorini discloses such a deposition temperature for a movable MEMS element formed after an integrated transistor.

It is thus respectfully submitted that claim 1 is patentable over the combination of Franke and Fiorini.

Claims 6-8 depend on claim 1, and are thus patentable over the combination of Franke and Fiorini at least for the same reasons that claim 1 is patentable.

Franke and Dreschel

Claims 9-10, 15, and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Franke in view of U.S. Patent No. 6,773,401 to Dreschel et al. ("Dreschel"). The rejection is respectfully traversed.

Claim 9 is patentable over the combination of Franke and Dreschel at least for reciting: "forming a capacitive micromachined ultrasonic transducer (CMUT) over the protective layer, the CMUT including a membrane that is formed using a high temperature process performed at a temperature of greater than 700°C, the plurality of transistors and the CMUT being formed on a same substrate." As explained above, Franke does not teach or suggest a process where a MEMS device is formed using a high temperature process greater than 700°C after integrated transistors have been formed.

Franke pertains to low temperature MEMS device processes, specifically processes lower than 650°C. Dreschel does not help Franke in this regard. Therefore, it is respectfully submitted that claim 9 is patentable over the combination of Franke and Dreschel.

Claims 10, 15, and 16 depend on claim 9, and are thus patentable over the combination of Franke and Dreschel at least for the same reasons that claim 9 is patentable.

Franke, Fiorini, and Dreschel

Claims 3 and 5 stand rejected under 35 U.S.C. §103 as being unpatentable over Franke in view of Fiorini as applied to claims 1, 6, 7, and 8 and further in view of Dreschel. The rejection is respectfully traversed.

Claims 3 and 5 depend on claim 1. The patentability of claim 1 over the combination of Franke and Fiorini has already been explained above. Dreschel does not add anything to Franke and Fiorini in regards to claim 1. Therefore, is respectfully submitted that claims 3 and 5 are patentable over the combination of Franke, Fiorini, and Dreschel at least for the same reasons that claim 1 is patentable.

Claims 11 and 12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Franke in view of Dreschel as applied to claims 9, 10, and 14-16 and further in view of Fiorini. The rejection is respectfully traversed.

As explained above, Franke, Fiorini, and Dreschel do not pertain to high temperature processing of MEMS movable elements, let alone formation of such movable elements at a temperature greater than 700°C after formation of integrated transistors. Therefore, it is respectfully submitted that claim 12 is patentable over the combination of Franke, Fiorini, and Dreschel.

De Samber and Hoshino

Claims 1, 6, and 7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,814,554 to De Samber et al. ("De Samber") in view of U.S. Patent No. 4,571,661 to Hoshino ("Hoshino"). The rejection is respectfully traversed.

Claim 1 is patentable over the combination of De Samber and Hoshino at least for reciting: "forming a first protective layer over a gate, source, and drain of the transistor." It is respectfully submitted that De Samber does not teach or suggest such a protective layer over a gate, source, and drain of a transistor. In De Samber, the cited silicon oxide ("protective layer") circumferentially covers the gate electrode 10 but not the drain and source of the transistor as required by claim 1 (De Samber, col. 3, lines 45-46).

Claim 1 is also patentable over the combination of De Samber and Hoshino at least for reciting: "forming a micro-electro-mechanical system (MEMS) structure over the first protective layer, the MEMS structure including a movable element that is formed using a deposition process at a temperature greater than about 700°C." According to the last office action, it would have been obvious to modify the teachings of De Samber so that its silicon nitride layer is deposited at about 700°C. Applicants respectfully disagree with this conclusion to the extent that it would degrade De Samber's device. De Samber FIG. 5 is reproduced below for ease of discussion.

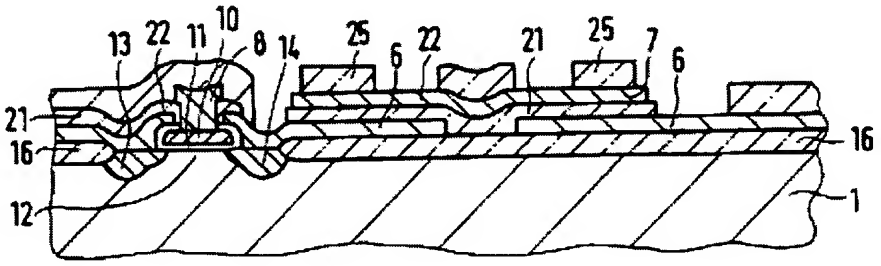

FIG.5

Referring to De Samber FIG. 5, deposition of portions 25 of silicon nitride at temperatures of about 700°C, as suggested in the last office action, exposes electrical connection 8 and other metals of the device to temperatures above their melting point. This is the exact situation warned by Franke (Franke, lines 39-43) and addressed by the

claimed invention. That is, one of ordinary skill in the art would not be motivated to deposit silicon nitride portions 25 at a temperature of about 700°C as that would lead to severe degradation of De Samber's device. Therefore, it is respectfully submitted that claim 1 is patentable over the combination of De Samber and Hoshino.

Claims 6 and 7 depend on claim 1, and are thus patentable over the combination of De Samber and Hoshino at least for the same reasons that claim 1 is patentable.

De Samber, Hoshino, Dreschel, and Franke

Claims 3, 5, and 8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over De Samber in view of Hoshino as applied to claims 1, 6, and 7 and further in view of Dreschel and Franke. The rejection is respectfully traversed.

Claims 3, 5 and 8 depend on claim 1. The patentability of claim 1 over the combination of De Samber and Hoshino has already been explained above. Dreschel and Franke do not add anything to the combination of De Samber and Hoshino in this regard. Therefore, is respectfully submitted that claims 3, 5, and 8 are patentable over the combination of De Samber, Hoshino, Franke, and Dreschel at least for the same reasons claim 1 is patentable.

De Samber, Dreschel, and Hoshino

Claims 9-12 and 14-16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over De Samber in view of Dreschel and Hoshino. The rejection is respectfully traversed.

Claim 9 is patentable over the combination of De Samber, Dreschel, and Hoshino at least for reciting: "forming a protective layer over the plurality of transistors after the plurality of transistors is formed." The last office action suggests that silicon oxide on De Samber's gate electrode 10 is the recited protective layer. It is respectfully submitted that De Samber does not teach or suggest such a protective layer over a plurality of transistors.

In De Samber, the cited silicon oxide circumferentially covers the gate electrode 10 but not the drain and source of the transistor as required by claim 1 (De Samber, col. 3, lines 45-46). In any event, such a gate oxide cannot possibly be formed over a plurality of transistors as required by claim 9.

Claim 9 is also patentable over the combination of De Samber, Dreschel, and Hoshino at least for reciting: "the CMUT including a membrane that is formed using a high temperature process performed at a temperature greater than 700°C." As explained above, De Samber cannot be modified to deposit a silicon nitride MEMS element at temperatures greater than 700°C as that would degrade De Samber's device.

Claims 10-12 and 14-16 depend on claim 9, and are thus patentable over the combination of De Samber, Dreschel, and Hoshino at least for the same reasons that claim 9 is patentable.

Hoshino and Franke

Claims 1, 9-12, and 14-16 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hoshino in view of Franke. The rejection is respectfully traversed.

Claim 1 is patentable over the combination of Hoshino and Franke at least for reciting: "forming a first protective layer over a gate, source, and drain of the transistor; and forming a micro-electro-mechanical system (MEMS) structure over the first protective layer, the MEMS structure including a movable element that is formed using a deposition process at a temperature greater than about 700°C."

The last office action proposes to modify the teachings of Hoshino and Franke such that a protective layer is formed over Hoshino's transistors. It is respectfully submitted that there is no motivation to combine Hoshino and Franke as they teach two completely different processes.

Firstly, there is no teaching in Hoshino or Franke how such a protective layer may be formed over Hoshino's transistors without interfering with the fabrication or operation of Hoshino's microstructure.

Secondly, the motivation to combine suggested by the last office action does not provide a reason why it would be desirable to perform the proposed combination. The last office action suggests that "it would be obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings by forming a protective layer over the transistor as taught by Franke et al. because the MEMS device can be indirectly connected to the transistor through the openings in the protective layer." It is respectfully submitted that the suggested motivation explains how to use a protective layer but not why the protective layer would be desirable in Hoshino's device. It is respectfully submitted that Hoshino has no use for such a protective layer over a transistor.

Thirdly, Franke's process involves a low temperature deposition process, which is incompatible with Hoshino's. In fact, Franke teaches away from using high temperature processes in the formation of MEMS structures (Franke, col. 1, lines 39-43). Therefore, there is no motivation for one of ordinary skill in the art to combine Hoshino and Franke to read on the present claims as Franke counsels against the method of claim 1. MPEP 2145(X)(D)(2) is explicit that it is improper to combine references where the references teach away from their combination. Here, Franke is explicit that MEMS structures should not be formed at high temperatures after an integrated transistor has been formed. Claim 1 is thus patentable over the combination of Hoshino and Franke.

Claim 9 is similarly patentable over the combination of Hoshino and Franke.

Claims 10-12 and 14-16 depend on claim 9, and are thus patentable over the combination of Hoshino and Franke at least for the same reasons that claim 9 is patentable.

Hoshino, Franke, and Dreschel

Claims 3, 5, and 8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hoshino in view of Franke as applied to claims 1, 9-12, and 14-16 and further in view of Dreschel. The rejection is respectfully traversed.

Claims 3, 5, and 8 depend on claim 1. The patentability of claim 1 over the combination of Hoshino and Franke has already been explained above. Dreschel does not add anything to Hoshino and Franke in regards to claim 1. Therefore, is respectfully submitted that claims 3, 5, and 8 are patentable over the combination of Hoshino, Franke, and Dreschel at least for the same reasons claim 1 is patentable.

Conclusion

For at least the above reasons, it is believed that claims 1, 3, 5-10, and 12-16 are in condition for allowance. The Examiner is invited to call the undersigned at (408)436-2112 for any question.

Respectfully submitted,
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